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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/774,230	01/30/2001	Rollie M. Fisher	199-1905 (VGT 0168 PUS)	1123

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EXAMINER	
HUYNH, KIM T	

ART UNIT	PAPER NUMBER
2112	6

DATE MAILED: 03/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/774,230	FISHER ET AL.	
	Examiner	Art Unit	
	Kim T. Huynh	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 January 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Nelson et al. (US Patent 6,138,185)

As per claim 1, Nelson discloses a controller for microprocessor input/output to at least one external device, said controller comprising:

- control logic; (col.5, lines 5-15)
- an input/output (I/O) crossover-switching network having a plurality of parallel pins; (col.7, lines 25-31)
- at least one serial I/O shifter in communication with said I/O crossover-switching network, said at least one serial I/O shifter having at least one channel; (col.3, line 37-col.4, lines 30)
- a clock signal for clocking a transfer of serial data from said controller to the external device; (col.5, lines 42-54), said clock signal for synchronizing the operation of said at least one serial I/O shifter; (col.2, lines 35-44), (col.4, lines 3-61)

- a latch signal for delimiting boundaries of transferred serial data; (col.4, lines 45-61)
- primary and secondary I/O signal pathways controlled by said I/O crossover-switching network for selecting I/O signals and usage of said plurality of parallel pins for communication with and control of the external device; and (col.3, line 37-col.4, line 44)
- wherein for said at least one channel, a first signal pathway is selectable between at least said primary signal pathway and said secondary signal pathway for connection to said at least one serial I/O shifter. (col.2, lines 25-44), (col.3, line 37-col.4, line 61)

As per claim 2, Nelson discloses the controller further comprising:

- optional signal pathways controlled by said I/O crossover-switching network for selecting I/O signals and usage of said plurality of parallel pins for communication with and control of the external device; and (col.3, line 37-col.4, line 61), (col.2, lines 25-44)
- wherein for said at least one channel, a second signal pathway is selectable between at least said primary signal pathway and said optional signal pathway for connection to a pin on the external device, said primary signal pathway being available to either said first signal pathway or said second signal pathway. (col.3, line 37-col.4, line 61)

As per claim 3, Nelson discloses the controller further comprising an external source for said clock and latch signals. (col.2, lines 52-54)

As per claims 4,9, 13, Nelson discloses the controller wherein said serial I/O shifter further comprises a high-speed serial shifter wherein serial data is transferred out of said shifter on one edge of said clock signal and transferred to said external device on the following edge of said clock signal. (col.4, lines 1-17)

As per claim 5, Nelson discloses a method for serializing parallel data comprising the steps of:

- sampling selected parallel I/O signals with a serial I/O shifter; (col.4, lines 1-30)
- selecting a signal path from a primary, secondary or optional signal path; (col.3, lines 37-61), (col.5, lines 17-28)
- serially transferring bits of the data stream from an I/O multiplexer to an external device at the rate of one bit per cycle of a clock signal; (col.4, lines 3-61), (col.9, lines 7-10)
- asserting a latch signal for enabling an external device; and (col.8, lines 58-67)
- outputting data as parallel I/O signals. (col.9, lines 11-19)

As per claim 6, Nelson discloses wherein said step of serially transferring bits of the data stream further comprises serially transferring bits at a rate of one bit per cycle of a clock signal. (col.4, lines 45-61)

As per claim 7, Nelson discloses wherein said step of sampling selected parallel I/O signals further comprises sampling selected parallel I/O signals on the leading edge of a latch signal to create a bit data stream. (col.4, lines 1-17)

As per claim 8, Nelson discloses wherein said step of outputting data further comprises setting a resolution of the parallel I/O signals using a frequency of the latch signal.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 10-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson et al. (US Patent 6,138,185) in view of Obata (US patent 6,301,509)

As per claim 10, Nelson discloses a method for parallel reconstruction of a serial data stream comprising the steps of:

- selecting a signal path from a primary, secondary or optional signal path; (col.4, lines 1-30), (col.3, lines 37-61), (col.5, lines 17-28)
- serially transferring bits of the data stream from an I/O multiplexer to an external device; (col.4, lines 45-61), (col.9, lines 7-10)
- outputting the parallel I/O signals to an I/O crossover-switching network; and (col.3, line 37-col.4, lines 30)
- asserting a latch signal for enabling another transfer of serial data from the external device. (col.8, lines 58-67)

Nelson discloses all the limitations as above except reconstructing the serial data into parallel I/O signals in a serial I/O shifter; However, Obata discloses a serial communication circuit interposed between the operation unit and the communication signal pattern for converting parallel signals output from the operation unit to serial signals and imparting the serial signals to the control input/output unit. (col.3, lines 24-32)

It would have been obvious to one having ordinary skills in the art at the time the invention was made to incorporate Obata's teaching into Nelson's system so as enable control input/output units to execute a plurality of functions, without degrading the performance of the programmable logic control system, in order to perform high-speed data communication. (col.1, lines 47-52)

As per claim 11, Nelson discloses wherein said step of serially transferring bits of the data stream further comprises serially transferring bits at a rate of one bit per cycle of a clock signal. (col.4, lines 45-61), (col.9, lines 7-10)

As per claim 12, Nelson discloses wherein said step of outputting data further comprises setting a resolution of the parallel I/O signals using the number of serial bits transferred, clock speed and the assertion of a latch signal. (col.9, lines 20-45)

Response to Amendment

5. Applicant's amendment filed on 12/23/03 have been fully considered but are not place application in condition for allowance.

a. In response to applicant's argument Nelson's reference does not teach or suggest clock signal for synchronizing the operation of said at least one serial I/O shifter. As Nelson notes at (col.4, lines 3-67) serial requests and serial responses can be processed concurrently which means processed during a single clock cycle. It is inherently disclose clock signal synchronizing operation of I/O switch 200. Furthermore, as Nelson notes at (col.2, lines 35-44), the first and second connection requests are concurrently processed. Thus, the prior art teaches the invention as claimed and the amended claims do not distinguish over the prior art as applied.

b. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, In this case, Examiner relies on Obata's reference the teaching of reconstructing the serial data into parallel I/O signals in a serial I/O shifter. As Obata notes at (col.3 lines 24-32) it is well established in the art to provide a serial communication circuit interposed between the operation unit and the communication signal pattern for converting parallel signals output from the operation unit to serial signals and imparting the serial signals to the control input/output unit. In that (col.1, lines 47-52), Obata's purpose is to provide control system which enables control input/output units to execute a plurality of

functions without degrading the performance of the control system, in order to perform high-speed data communication. It is clear that Obata is analogous art and therefore properly combinable for the purpose stated in the rejection of record.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (703)305-5384 or via e-mail addressed to [kim.huynh3@uspto.gov]. The examiner can normally be reached on M-F 8:30AM- 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on (703) 305-4815 or via e-mail addressed to [mark.rinehart@uspto.gov]. The

fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9306 for regular communications and After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)306-5631.

Kim Huynh

Feb. 25, 2004

Khanh Dang
Primary Examiner